2827

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

IN THE MATTER OF:

GROUP: 2827

H/A
J. Steptoe
10-17-02

Jin Chuan BAI

SERIAL NO.: 09/921,150

EXAMINER: ZARNEKE, David A.

FILED: August 2, 2001

FOR: PACKAGING PROCESS FOR SEMICONDUCTOR PACKAGE

AMENDMENT

Assistant Commissioner of Patents
& Trademarks
Washington, DC 20231

S I R:

This is in response to the outstanding office communication dated July 3, 2002. Any necessary fees should be deducted from Deposit Account No. 01-1944.

IN THE CLAIMS:

Please substitute the attached claim 1 for claim 1 of record. A copy of claim 1 as amended and a copy of claim 1 showing the amendments thereto is attached.

Also attached hereto is a certified copy of the priority document as required under 35 USC 119(b).

REMARKS

Applicant has submitted the certified copy of the Taiwan parent patent application upon which this application is based. Accordingly, applicant's claim for foreign priority under 35 USC 119(b) based upon this application is now believed to be perfected.

The objection to claim 1 has been noted and the suggested correction has been adopted. Accordingly, the objection to claim 1 should now be withdrawn.

Applicant wishes to note that the Examiner has rejected claims 1-8 under 35 USC 103(a) but has attached the heading "Claim Rejections - 35 USC 102" which does not apply to the rejection under 35 USC 103. Nevertheless, applicant will assume that a rejection under 35 USC 103(a) was intended and not under 35 USC 102.

The rejection of claims 1-8 under 35 USC 103(a) as being unpatentable over Ito, et al (U.S. Patent 6,333,206) in view of applicant's admitted prior art and Chen, et al (U.S. Patent 6,262,264) or Nguyen, et al (U.S. Patent 6,245,595) or Wang, et al (U.S. Patent 6,168,972) or Urushima (U.S. Patent Publication 2001/0036711) is respectfully traversed.

Applicant has amended claim 1 to emphasize that the first encapsulant has a top surface formed in coplanar alignment with flat ends of the conductive elements to thereby form a common, coplanar surface and with at least one semiconductor chip prepared such that the plurality of bond pads are formed on a surface for mounting the semiconductor chip on the top surface of the first encapsulant to cause the bond pads to be electrically connected to the exposed ends of the conductive elements. The surface of the semiconductor chip is closely attached to the coplanar surface formed by the first encapsulant such that the conductive elements are free of any gaps between the semiconductor chip and the coplanar surface.

Applicant's invention is directed to a packaging process for a semiconductor package in which a plurality of conductive elements (conductive bumps) are disposed on a chip-mounting area of a substrate with each conductive element having a flat end. A first encapsulant is formed on the substrate to encapsulate the conductive elements, and a top surface of the first encapsulant is adapted to be coplanarly aligned with the flat ends of the conductive elements so as to form a coplanar surface with the exposed ends of the conductive elements. Thereafter, at least a chip (flip chip) is

mounted on the top surface of the first encapsulant, allowing bond pads formed on the chip to be electrically connected to the exposed ends of the conductive elements. A second encapsulant is then formed on the substrate to encapsulate the chip. Compared to the admitted prior art of mounting a flip chip on a substrate first and then performing an underfill process to fill a chip-substrate gap, the packaging method of the subject invention eliminates problems of voids and popcorn effect.

Ito, et al ('206) discloses a process for producing a semiconductor device. In the embodiment of column 10, lines 40-57 (Figs. 6 and 7), an underfill resin layer 13 is formed on a surface of a printed circuit board 1 having a plurality of spherical connecting electrode portions (joint balls) 2 located thereon in an arrangement such that the top of the connecting electrode portions 2 are exposed and protrude from the resin layer 13. Then, a semiconductor element 3 is placed on the printed circuit board 1, allowing the exposed/protruded connecting electrode portions 2 to be in contact with electrode portions of the semiconductor element 3. This causes a gap to be formed between the semiconductor element 3 and the resin layer 13, as shown in Fig. 7. Thereafter, a heating process is performed to melt the resin layer 13, which is pressed to fill the gap between the semiconductor element 3 and the resin layer 13. After that, the resin layer 13 is hardened and cured.

In comparison, the subject invention uses conductive elements with flat ends, wherein the first encapsulant is flush with the flat ends to form a common coplanar surface. In this way, a chip can be directly attached to the coplanar surface without leaving any gaps between the chip and the first encapsulant or conductive elements, eliminating the steps of heating to melt resin for gap-filling and then curing the resin as in Ito, et al.

Chen, et al ('264), Wang, et al ('972) and Urushima (2001/0036711) all teach a plurality of spherical conductive bumps on a substrate with the conductive bumps encapsulated by a resin material. Thereafter, the resin material and the conductive

bumps are partially removed to expose the conductive bumps. The conductive bumps are then adapted to form flat ends. This is different from the process of the present invention in which the conductive elements are inherently formed with flat ends before encapsulation..

Nguyen, et al ('595) teaches the necessity to flatten solder bumps during a molding process through the use of a mold as explained in column 4, lines 39-65 (Figs. 2 and 3). A wafer 100 having a plurality of solder balls 108 is placed within a lower mold cavity 200. A compliant release film 206 is then placed on the solder bumps 108, and an upper portion 208 of the mold 202 is applied to exert a pressure on the film 206 to thereby flatten the solder bumps 108 so as to allow an underfill encapsulant 210 to be readily injected into the mold 202. In the present invention there is no need to perform bump-flattening during molding nor is there a need to use an encapsulating mold to flatten the solder bumps.

For all the above reasons, the rejection of claims 1-8 under 35 USC 103 should be withdrawn.

Reconsideration and allowance of claims 1-8 is respectfully solicited.

Respectfully submitted,

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MAILING CERTIFICATE

I hereby certify that this correspondence is being deposited with the U.S. Postal Service as first class mail in an envelope addressed: Commissioner of Patents & Trademarks, Washington, DC 20231 on October 3, 2002.

Date: Oct-3, 2002